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APPLICATION NO. FILING DATE		LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/016,772	12/10/2001		Robert Thomas Bailis	RPS920010126US1 3353		
25299	7590	01/24/2003				
IBM CORPO		N	EXAMINER			
PO BOX 1219 DEPT 9CCA,	-	002		CHANG, D	CHANG, DANIEL D	
		LE PARK, NC	27709			
				ART UNIT	PAPER NUMBER	
				2819		
				DATE MAILED: 01/24/2003	DATE MAILED: 01/24/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
\	10/016,772	BAILIS ET AL.					
Office Action Summary	Examiner	Art Unit					
	Daniel D. Chang	2819					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).  Status							
1) Responsive to communication(s) filed on 15 A	A <u>pril 2002</u> .						
2a) This action is <b>FINAL</b> . 2b)⊠ Thi	is action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. <b>Disposition of Claims</b>							
4) Claim(s) 1-11 is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-11</u> is/are rejected.	6)⊠ Claim(s) <u>1-11</u> is/are rejected.						
7) Claim(s) is/are objected to.	7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.							
Application Papers							
9) The specification is objected to by the Examiner.							
10)⊠ The drawing(s) filed on <u>28 February 2002</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.							
If approved, corrected drawings are required in reply to this Office action.							
12)☐ The oath or declaration is objected to by the Examiner.							
Priority under 35 U.S.C. §§ 119 and 120							
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a) ☐ All b) ☐ Some * c) ☐ None of:							
1. Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents	2. Certified copies of the priority documents have been received in Application No						
<ul> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>							
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).							
a) The translation of the foreign language provisional application has been received.  15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.							
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4	5) Notice of Informal	y (PTO-413) Paper No(s) Patent Application (PTO-152)					

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### Specification

The disclosure is objected to because of the following informalities: on pages 1-2, blank lines should be filled with serial numbers. Appropriate correction is required.

#### Claim Objections

Claims 4, 6 and 10 are objected to because of the following informalities: In claim 4, line 4, between "coupled" and "the", the word --to-- or --between-- should be entered. In claim 6, line 3, "a" before "at least" should be deleted. In claim 10, line 7, "a" before "plurality" should be changed to --the--. Appropriate correction is required.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Agrawal et al. (US 5,260,881).

Regarding claims 1-7, Agrawal discloses, in figures 1 and 61-64, an ASIC (programmable gate array shown in fig. 1) comprising:

a standard cell (CLBs R1C1-R8C8); a plurality of input output pins (pins connected to IOB 1-110); and at least one FPGA interconnect (PIPs and/or connection to MUX in IOB shown in figures 61-64; see col. 41, lines 21+) coupled to the plurality of I/O pins and the plurality of

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logic functions, wherein the at least one FPGA interconnect can be configured to select one of the plurality of logic functions (see fig. 16A) utilizing field programming techniques (see PIP in fig. 17); and wherein the one logic function is coupled to an internal bus (see 15 in fig. 16a) via the at least one configured FPGA interconnect.

Regarding claims 8 and 9, utilizing at least one FPGA interconnect to correct wiring error which is a reversed bit order wiring error, when the ASIC is utilized on a printed circuit board, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Regarding claims 10 and 11, Agrawal discloses, in figures 1 and 61-64, an ASIC (programmable gate array shown in fig. 1) comprising:

- a plurality of I/O pins (pins connected to IOB 1-28);
- a plurality of first logic functions (CLBs R1C1-R1C8 or R2C1-R2C8);
- a first FPGA interconnect (PIPs and/or connection to MUX in IOB shown in figures 61; see col. 41, lines 21+) coupled between the plurality of I/O pins and the plurality of first logic function, wherein the first FPGA interconnect can be configured to select at least one of the plurality of first logic functions (see fig. 16A);
  - a bus (HBUS1) coupled to the plurality of first logic functions;
- a second FPGA interconnect (segment box or switch matrix or PIPs in HBUS1 or HBUS2) coupled between the bus and the plurality of first logic functions, wherein the second FPGA interconnect is configured to connect to one of the plurality of first logic functions to the bus; and

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a plurality of second logic functions (CLBs R3C1-R3C8) coupled to the bus.

#### Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

> Daniel D. Chang **Primary Examiner**

> > DANIEL CHANG

POSSEY EXAMINER

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DC January 16, 2003